Notice of Allowability	Application No.	Applicant(s)	
	10/781,782	YAMASHITA ET AL.	
	Examiner	Art Unit	
	VIJAY SHANKAR	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2-20-2004*.

2. ☒ The allowed claim(s) is/are *1-42*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

VIJAY SHANKAR
Primary Examiner
Art Unit: 2629

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Allowable Subject Matter

2. Claims 1-42 are allowed.

3. The following is an examiner's statement of reasons for allowance: The prior arts fails to teach a display device comprising **a control circuit for generating at least a clock signal and an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of the monitor line, and correcting the timings of generation of at least the clock signal and inverse clock signal based on the change of the timing of the potential change; a horizontal scanner; a first monitor circuit; and a second monitor circuit, wherein the horizontal scanner includes: a shift register, in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with the clock signal and inverse clock signal at the time of the first scanning operation or the time of the second scanning operation, a first switch group for alternately sequentially sampling the**

clock signal and inverse clock signal in response to the shift pulses output from the corresponding shift stages of the shift register and outputting them as sample-and-hold pulses, and a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of the first switch group and supplying them to the corresponding signal lines of the pixel portion, the first monitor circuit includes: a shift stage which is connected to the last shift stage of the shift register in the horizontal scanner at the time of the first scanning operation and outputs the shift pulses in synchronization with the clock signal and inverse clock signal when performing shift-in of the signal by the last shift stage, a third switch for sampling signals-different from the signal sampled from the last shift stage among the clock signal and inverse clock signal in response to the shift pulse output from the shift stage and outputting the same as the sample-and-hold pulses, and a fourth switch for setting the potential of the monitor line at a second potential in response to the sample-and-hold pulses from the third switch, and the second monitor circuit includes: a shift stage which is connected to the initial shift stage of the shift register in the horizontal scanner at the time of the second scanning operation-and outputs the shift pulses in synchronization with the clock signal and inverse clock signal when performing the shift-in of the signal by the initial shift stage, a fifth switch for sampling signals different from that of the signal sampled from the initial shift stage among the clock signal and inverse clock signal in response to the shift pulses output from the shift stage and outputting the same as the sample-and-hold pulses, and

a sixth switch for setting the potential of the monitor line at the second potential in response to the sample-and-hold pulses from the fifth switch as claimed in Claim 14.

4. The prior arts fails to teach a display device comprising: **an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of the monitor line, and correcting the timings of generation of at least the clock signal and inverse clock signal based on the change of the timing of the potential change; a horizontal scanner; and a monitor circuit, wherein the horizontal scanner includes: a shift register, in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with the clock signal and inverse clock signal at the time of the first scanning operation or the time of the second scanning operation, a first switch group for alternately sequentially sampling the clock signal and inverse clock signal in response to the shift pulses output from the corresponding shift stages of the shift register and outputting them as sample-and-hold pulses, and a second switch group for sequentially sampling video signals-in response to the sample-and-hold pulses from the switches of the first switch group and supplying them to the**

corresponding signal lines of the pixel portion, and the monitor circuit includes: a selector portion for receiving the switch signal, sampling signals different from the signal sampled by the first shift stage of the shift register in the horizontal scanner among the clock signal and inverse clock signal when the switch signal indicates the first scanning operation and sampling signals different from the signal sampled by the last shift stage of the shift register in the horizontal scanner among the clock signal and inverse clock signal when the switch signal indicates the second scanning operation, and outputting the same as the sample-and-hold pulses, and a third switch for setting the potential of the monitor line at a second potential in response to the sample-and-hold pulses from the selector portion as claimed in Claim 1.

5. The prior arts fails to teach a projection type display device comprising an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of the monitor line, and correcting at least the timings of generation of the clock signal and inverse clock signal based on the change of the timing of the potential change; a display panel including a pixel portion in which a plurality of pixels are arrayed in a matrix and signal lines are laid for every pixel column, a horizontal scanner, and a monitor circuit; an irradiating means for irradiating the light to the display panel; and a projecting means for projecting light passing through the display panel, wherein the horizontal scanner of the display panel includes: a shift

register in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with the clock signal and inverse clock signal at the time of the first scanning operation or the time of the second scanning operation, a first switch group for alternately sequentially sampling the clock signal and inverse clock signal in response to the shift pulses output from the corresponding shift stages of the shift register and outputting them as sample-and-hold pulses, and a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of the first switch group and supplying them to the corresponding signal lines of the pixel portion, and the monitor circuit of the display panel includes: a selector portion for receiving the switch signal, sampling signals different from the signal sampled by the first shift stage of the shift register in the horizontal scanner among the clock signal and inverse clock signal when the switch signal indicates the first scanning operation and sampling signals different from the signal sampled by the last shift stage of the shift register in the horizontal scanner among the clock signal and inverse clock signal when the switch signal indicates the second scanning operation, and outputting the same as the sample-and-hold pulses, and a third switch for setting the

potential of the monitor line at a second potential in response to the sample-and-hold pulses from the selector portion as claimed in Claim 22.

6. The prior arts fails to teach a projection type display device comprising **an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of the monitor line, and correcting at least the timings of generation of the clock signal and inverse clock signal based on the change of the timing of the potential change; a clock generation circuit for generating a second clock signal and a second inverse clock signal having the same period as the first clock signal and first inverse clock signal and having a small duty ratio based on the first clock signal and first inverse clock signal generated at the control circuit; a display panel including at least a pixel portion in which a plurality of pixels are arrayed in a matrix and signal lines are laid for every pixel column, a horizontal scanner, and a monitor circuit; an irradiating means for irradiating light to the display panel; and a projecting means for projecting the light passed through the display panel onto a screen, wherein the horizontal scanner of the display panel includes: a shift register, in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with the**

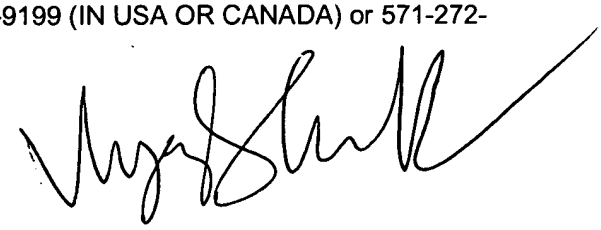
clock signal and inverse clock signal at the time of the first scanning operation or the time of the second scanning operation, a first switch group for alternately sequentially sampling the second clock signal and second inverse clock signal in response to the shift pulses output from the corresponding shift stages of the shift register and outputting them as sample-and-hold pulses, and a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of the first switch group and supplying them to the corresponding signal lines of the pixel portion, and the monitor circuit of the display panel includes: a selector portion for receiving the switch signal, sampling signals having different phases from that of the signal sampled by the first shift stage of the shift register in the horizontal scanner between the first clock signal and first inverse clock signal when the switch signal indicates the first scanning operation and sampling signals having different phases from that of the signal sampled by the last shift stage of the shift register in the horizontal scanner between the first clock signal and first inverse clock signal when the switch signal indicates the second scanning operation, and outputting the same as the sample-and-hold pulses, and a third switch for setting the potential of the monitor line at a second potential in response to the sample-and-hold pulses from the selector portion as claimed in Claim 29.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



VIJAY SHANKAR
Primary Examiner
Art Unit 2629

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